REMARKS/ARGUMENTS

Claims 11-20 and 22-34 are pending in this application. By this Amendment, Applicants amend claims 14, 15 and 23.

Claims 11-20 and 22-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Buckelew et al. (U.S. 6,667,744) in view of Vainsencher (U.S. 5,977,997). Applicants respectfully traverse this rejection.

Claim 14 has been amended to recite:

> "An apparatus for image processing, comprising:
> a processor including a data decompression circuit;
> **a first storage device having texture data and electronically coupled to said processor**; and
> **a texture buffer having decompressed texture data and electrically coupled to said processor**; wherein
> transmission of texture data between said texture buffer and said processor is faster than transmission of texture data between said storage device and said processor; and
> **said first storage device is defined by a CPU work memory or an external memory device.**" (emphasis added)

Claims 15 and 23 recite features that are similar to the features recited in claim 14, including the above-emphasized features.

The Examiner alleged that Buckelew et al. teaches an apparatus (and method) for image processing including all of the features and method steps recited in claims 14, 15 and 23, except for the inclusion of a data decompression circuit. The Examiner further alleged that Vainsencher teaches a processor including a data compression circuit. Thus, the Examiner concluded that it would have been obvious "to modify BUCKELEW et al. by VAINSENCHER because both inventions share similar technological environments corresponding to graphics and video processing in single chip computer systems." Applicants respectfully disagree.

First, the Examiner alleged that elements 114 and 116 of Buckelew et al. correspond to the first storage device and the texture buffer recited in Applicants' claimed invention. This is clearly incorrect. Element 114 of Buckelew et al. is disclosed

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as being a texture buffer and element 16 of Buckelew et al. is disclosed as being a frame buffer. More particularly, Buckelew et al. specifically discloses that the frame buffer 116 stores pixel colors and that the frame buffer 116 "has a full set of planes for each pixel. Each plane for each pixel represents information being tracked for that pixel. Planes are logically bundled into sets. The three most common plane sets are red, green, and blue, representing the pixel's display color. . . ." (see, for example, col. 12, lines 41-57).

Buckelew et al. neither teaches nor suggests that the frame buffer could or should include texture data. Thus, Applicants respectfully submit that the frame buffer 116 of Buckelew et al. cannot be fairly construed as either of the first storage device or the texture buffer as recited in Applicants' claimed invention. At best, Buckelew et al. teaches **only one** element (texture buffer 114) for storing texture data, and certainly fails to teach or suggest the features of "a first storage device having texture data and electronically coupled to said processor" **and** "a texture buffer having decompressed texture data and electrically coupled to said processor" as recited in Applicants' claimed invention.

Second, even assuming *arguendo* that the texture buffer 114 and the frame buffer 116 of Buckelew et al. could be fairly construed as the first storage device and the texture buffer recited in Applicants' claimed invention, neither the texture buffer 114 nor the frame buffer 116 of Buckelew et al. is defined by either of a CPU work memory or an external memory device, but rather, both the texture buffer 114 and the frame buffer 116 of Buckelew et al. are merely defined by a buffer memory. Thus, Buckelew et al. clearly fails to teach or suggest the feature of "said first storage device is defined by a CPU work memory or an external memory device" as recited in Applicants' claimed invention.

Vainsencher is relied upon merely to teach a decompression circuit. Vainsencher clearly fails to teach or suggest the features of "a first storage device having texture data and electronically coupled to said processor," "a texture buffer having decompressed texture data and electrically coupled to said processor" and "said

first storage device is defined by a CPU work memory or an external memory device" as recited in Applicants' claimed invention.

The Examiner alleged that the motivation to modify the apparatus of Buckelew et al. as taught by Vainsencher would have been "because both inventions share similar technological environments corresponding to graphics and video processing in single chip computer systems." Applicants respectfully submit that this is clearly insufficient motivation to combine Vainsencher with Buckelew et al.

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Prior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantage to be derived from combining their teachings. In re. Sernaker, 217 USPQ 1 (Fed. Cir. 1983).

First, the Examiner's has failed to even allege that **any** advantage would have been obtained by modifying the apparatus of Buckelew et al. to include the decompression circuit of Vainsencher. The mere fact that two inventions might "share similar technological environments" would certainly not motivate one of ordinary skill in the art to combine the teachings thereof.

Second, Vainsencher fails to teach or suggest that the decompression circuit disclosed therein could or should be used in an apparatus as disclosed in Buckelew et al.

Third, since the apparatus of Buckelew et al. performs all of the objectives thereof **without** a decompression circuit, there would have been absolutely no reason to include the decompression circuit of Vainsencher therein. In fact, if the decompression circuit of Vainsencher were included in the apparatus of Buckelew et al., the combination and arrangement of circuit elements of Buckelew et al. would have to be completely modified and rearranged in order to perform the objectives disclosed therein.

Thus, Applicants respectfully submit that there would have been absolutely no motivation to combine the teachings of Vainsencher with Buckelew et al.

Accordingly, Applicants respectfully submit that Buckelew et al. and Vainsencher, applied alone or in combination, fail to teach or suggest the unique combination and

arrangement of features and/or method steps recited in Applicants' claims 14, 15 and 23.

In view of the foregoing amendments and remarks, Applicants respectfully submit that Claims 14, 15 and 23 are allowable. Claims 16-20, 22 and 24-34 depend upon claims 14, 15 and 23, and are therefore allowable for at least the reasons that claims 14, 15 and 23 are allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicants petition the Commissioner for a One-month extension of time, extending to June 12, 2004, the period for response to the Office Action dated February 12, 2004.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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Attorneys for Applicant

Joseph R. Keating
Registration No. 37,368

Christopher A. Bennett
Registration No. 46,710

KEATING & BENNETT LLP
10400 Eaton Place, Suite 312
Fairfax, VA 22030
Telephone: (703) 385-5200
Facsimile: (703) 385-5080

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